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VHDL IMPLEMENTATION OF DS SS-CDMA TRANSMITTER AND RECEIVER FOR AD HOC NETWORK

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Abstract- in past few years, lot of research is performed in both industries and academics into the development of CDMA. In DS-SS CDMA multiple signal channels occupy the same frequency band being distinguished by the use of different spreading codes. Digital cellular telephone system and personal communication system uses CDMA communication. In this project direct sequence spread spectrum principle based code division multiple access (CDMA) transmitter and receiver is implemented in VHDL for FPGA. The transmitter module mainly consists of data generator, programmable chip sequence generator (PN sequence generator), direct digital frequency synthesizer (DDFS), BPSK modulator blocks. The receiver modular mainly consists of BPSK demodulator, programmable chip sequence generator (PN sequence generator), matched filters, threshold detector blocks. Modelsim Altera 13.1 tool will be used for functional and logic verification at each block. The Xilinx synthesis technology of Xilinx ISE 9.2i tool will be used for synthesis of transmitter and receiver on FPGA Spartan 3E. A transmitter and Receiver components have been designed individually using Bottom-up approach. The designs then are combined and defined by component declaration and port mapping. This project concentrates on application of VHDL simulation and FPGA compiler to Wireless Data components.

Index Terms- DS-SS, BPSK modulator and demodulator, DSSS, FPGA, PN sequence generator.

I. INTRODUCTION

Direct sequence code division multiple access (DS-CDMA) technique allows improved privacy and security, increased capacity. Also it is spectrally efficient and high quality digital cellular system. VHDL implementation of DS-CDMA transmitter and receiver has been proposed in this project.

This project implements DS-CDMA transmitter and receiver through VHDL. Every mobile handset and every wireless base station operates on the same frequency spectrum .For the discrimination of one conversation from the other, every handset broadcast a unique code sequence is called as pseudo noise code. Here pseudo noise code is generated by using two six bit LFSRs. Code signal is called as chip signal. The chips modulated by the carrier using a digital modulation technique BPSK. The carrier is generated using discrete digital frequency synthesizer.

CDMA base stations must be able to discriminate this different code sequences in order to distinguish one transmission from other. This discrimination is accomplished by means of a matched filter. A matched filter is a filter whose frequency spectrum is exactly designed to match the frequency spectrum of the input signal. Here matched filter generating the pseudo noise code, generated noise code is correlated with the received code and detecting original data.

In the recent years the CDMA on FPGA platform has attracted attention of academic research and industry. The Spartan TM-3E family of Field-Programmable Gate Arrays (FPGAs) is specifically broadband designed to meet the needs of high volume, cost-sensitive consumer electronic applications. The five-member family offers densities ranging from 100,000 to 1.6 million system gates. Because of their exceptionally low cost, Spartan -3E FPGAs are ideally suited to a wide range of consumer electronics applications, including access, home networking, display/projection, and digital television equipment.

II. MULTIPLE ACCESS TECHNIQUES

Multiple Access method allows many simultaneous users to use the same fixed bandwidth frequency spectrum. For mobile phone systems the total bandwidth is typically 50 MHz, which is split in half to provide the forward and reverse links of the system. Sharing of the spectrum is required in order to increase the user capacity of any wireless network. FDMA, TDMA and CDMA are the three major methods of sharing the available bandwidth to multiple users in wireless system. Among these multiple access techniques CDMA provides less interfered and more secured type communication hence is more important. A. Frequency Division Multiple Access

In Frequency Division Multiple Access available bandwidth is subdivided into a number of narrower band channels. Each user gets a unique frequency band for transmitting and reception. During a call, no other user can use the same frequency band. Each user is allocated a forward link channel (from the base station to the mobile phone) and a reverse channel (back to the base station), each being a single way link. The transmitted signal on each of the channels is continuous allowing analog transmissions. The channel bandwidth used in most FDMA systems is typically low (30 kHz) and channel only support a single user.

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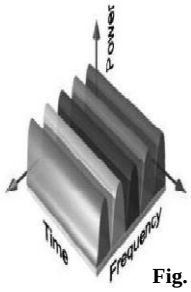

Fig. 1 FDMA

B. Time Division Multiple Access

Time Division Multiple Access (TDMA) divides the available spectrum into multiple time slots, by giving each user a time slot in which they can transmit or receive TDMA systems Transmit data in a buffer and burst method, thus the transmission of each channel is non-continuous. The input data to be transmitted is buffered over the previous frame and burst transmitted at a higher rate during the time slot for the channel. TDMA cannot send an analog signal directly due to the buffering required, thus is only used for transmitting.

C. Code Division Multiple Access

Code Division Multiple Access (CDMA) is a spread spectrum technique that uses neither frequency channels nor time slots. With CDMA, the narrow band message (typically digitized voice data) is multiplied by a large bandwidth signal that is a pseudo random noise code (PN code). All users in a CDMA system use the same frequency band and transmit simultaneously. The transmitted signal is recovered by correlating the received signal with the PN code used by the transmitter.

CDMA technology was originally developed by the military during World War II. Researchers were spurred into looking at ways of communicating that would be secure and work in the presence of jamming. Some of the properties that have made CDMA useful are:

Anti-jam and interference rejection
Information security
Accurate Ranging

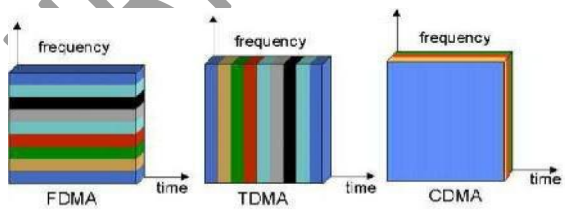

Fig. 2 Types of Multiple Access Schemes.

III. SPREAD SPECTRUM TECHNIQUES

Based on the modulation method the CDMA technique can be classified into three categories.
CDMA: frequency hopping (FH)
CDMA: direct sequence (DS)

A. Frequency hopping spread spectrum

The signal is broadcasted over a random series of radio frequencies, hopping from one frequency to another frequency at fixed intervals a receiver, hopping between frequencies in synchronization with the transmitter picks up the message.

B. Direct sequence spread spectrum

DS-CDMA is achieved by spreading the data signal by a pseudo random noise sequence (PN code), which has a chip rate higher than the bit rate of the data. The PN code sequence is a sequence of ones and zeros (called chips), which alternate in a random fashion. The PN code used to spread the data can be of two main types. A short PN code (typically 10-128 chips in length) can be used to modulate each data bit. The short PN code is then repeated for every data bit allowing for quick and simple synchronization of the receiver. Alternatively a long PN code can be used. In DS-CDMA the spreaded signal is modulated by a RF carrier. For the modulation, various modulation techniques can be used, but usually some form of phase shift keying (PSK) like binary phase shift keying (BPSK), differential binary phase shift keying (D-BPSK), quadrature phase shift keying (QPSK), or minimum shift keying (MSK) is employed.

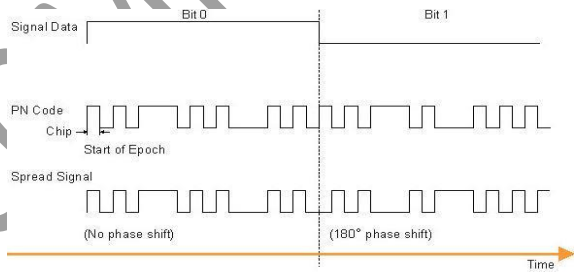

Fig. 3 Direct sequence signals

In DS-CDMA the data signal is directly modulated by a digital, discrete time, discrete valued code signal from this direct multiplication that the direct sequence CDMA gets its name.

IV. HARDWARE AND SOFTWARE DESIGN AND IMPLEMENTATION

A. Specifications

1. Type of PN Sequence: Gold Code
2. LFSR Size: Two 7 bit LFSRs in case of Gold Sequence
3. PN Sequence Length: 127 in case of gold sequence
4. Maximum no. of communication Links: 63 in case of gold sequence
5. Type of Correlator: Matched Filter.
6. Type of Signal Synthesis: LUT based direct digital frequency
7. Type of Modulation: BPSK
8. Type of demodulation: Coherent BPSK demodulation

B. Synthesis

9. Phase Resolution in DDFS : 5.625

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10. Threshold Type adjustable: Constant Threshold value.
11. Front end Design Entry : VHDL
12. Backed Synthesis : Xilinx Spartan III FPGA
13. Tools used while developing, testing, implementing and programming the CDMA transmitter and receiver blocks. Simulation - Modelsim ALTERA 13.1 Edition Synthesis - Xilinx Synthesis Technology (XST) of Xilinx ISE

C. CDMA Transmitter

In CDMA transmission user data is spreaded by a PN sequence and then modulated using BPSK modulation where in the carrier is generated using digital frequency synthesizer principle .Then the modulated signals from different users are combined and transmitted.

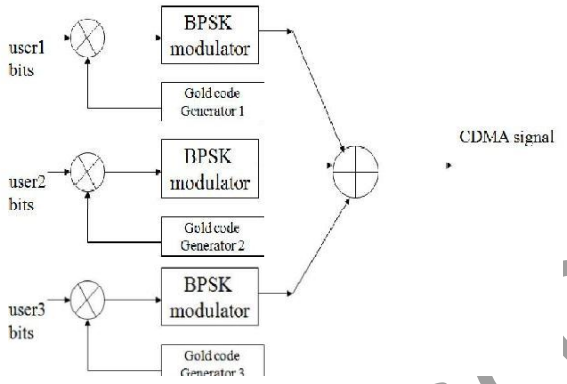

Fig.4. Block diagram of multiple user CDMA transmitters

The main blocks of CDMA transmitter are listed below.

1) Clock distributor
2) PN sequence generator
3) Signal spreader
4) BPSK modulator

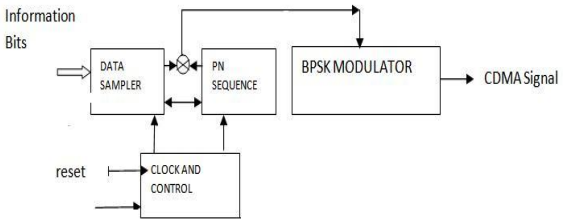

Fig.5 Block diagram of CDMA transmitter.

A. Clock Distributer

The clock distributor derives different clock signals from master clock, which are required for Spread spectrum signal generation.

B. PN Sequence Generation

PN sequence generator is the important block of DS-CDMA communication system. The PN sequence generator can be implemented using LFSRs to generate several types of PN sequences. Two types of PN sequence generators implemented in this project. They are ML sequences and gold codes.

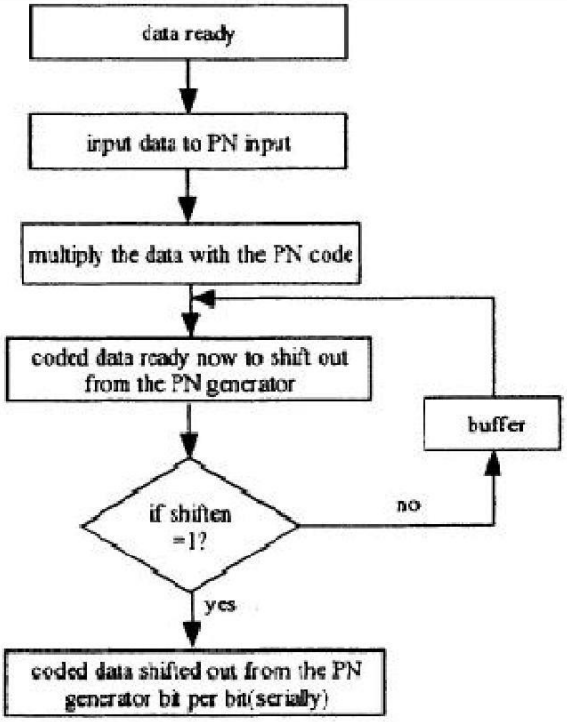

Fig.6. the flow chart of the PN generator

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LFSR based maximal length sequence produce the maximum possible length sequence. For n bit size shift registers the PN sequence length will be 2n-1 bit. Here 6 bit LFSR is implemented. Length of ml sequence generated is 63.Number of communication links that can be supported is 63.

C. Gold Sequence Generator

Length of gold sequence generated is 127 Number of communication links supported is a 63.Correlation property of gold sequences is better than ml sequences and hence they are more preferred.

D. Signal Spreader

The function of signal spreader is to generate PN sequence when the information bit is "1". and generate the complement of the PN sequence if the information bit is "0". For this we use XOR gate controlled inverter action. The spreaded chip signal is used for modulation by BPSK modulator.

E. BPSK Modulator

The BPSK modulator produces the band pass spread spectrum signal which is suitable for transmission from the spreaded signal. The BPSK modulator is implemented using pure digital architecture. The Direct Digital Frequency Synthesis (DDFS) technique with phase shifting provision is used for the signal generation.

D. CDMA RECEIVER

The CDMA receiver gets its input from the transmitter section and recovers the data using matched filter. The matched filter can distinguish the PN sequence and the passes the data to the respective user

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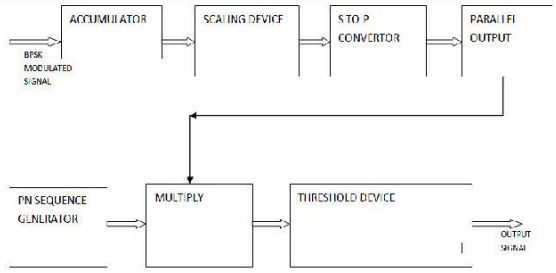

Fig.7: Block diagram of CDMA Receiver

The receiver performs the following steps to extract the Information:
Demodulation
Accumulation
Scaling
Serial to parallel conversion Multiplying and dispreading Threshold device

A. BPSK demodulator

BPSK demodulator receives the DS-CDMA signals. The BPSK demodulator produce 15 (-7 to 7) digital words, unlike in conventional BPSK demodulator which produces only two symbols ("1" and "0"). This is necessary due to the low power spectral density of DS-CDMA signals and it is only possible to detect the information bits after correlation.

B. Multiplier

Multiplies the incoming signal with the LO output. The multiplication is performed in 2s complement and the 15 bit result is given to the accumulator.

C. Local oscillator

The Local oscillator produces 6 bit signed bits representing the COS signal. The same principle DDFS which is used in transmitter is used in the receiver.

D. Accumulator

Functions as integrator in the analog equivalent. The accumulator accumulates the outputs of multiplier for one symbol duration and outputs at the beginning of next symbol.

E. Scaling device

The scaling device accepts the output of accumulator and scales its value to 4 bit signed number range, i.e., -7 to +7. This is done in order to reduce the complexity at the correlator and even at the hardware implementation level.

F. Serial to parallel converter

The serial to parallel converter accepts the outputs of the BPSK demodulator and produces parallel vector with an array of 128 words. This parallel 128 words constitute the most recent 128 outputs of the BPSK demodulator. This becomes input to the correlator.

G. PN sequence generator

In the receiver side the complete PN sequence is required every time for correlating with the outputs of BPSK demodulator it is provided as a parallel vector. Also "1" of PN sequence is provided as +1 and "0" is provided as -1, which is the required form for correlator.

H. Matched filter

Matched filter based correlator is used for receiving the DS-CDMA signals. The correlator accepts the 128 demodulator outputs and multiplies with 128 length PN sequence which is a sequence of +1 and -1. The outputs of multipliers are accumulated to produce the correlator output. The magnitude of the correlator output peaks whenever exact match occurs between the PN sequence and BPSK demodulator outputs. The output of the matched filter is given to the threshold detector, for detecting the information bits.

I. Threshold detector

The threshold detector compares the magnitude of the correlator output with the threshold value. If the magnitude of the correlator output is higher than the threshold value, then it raises a flag indicating that one bit is detected. If the sign of the correlator output is positive, then it will be interpreted as "1". Otherwise it will be declared as "0". The detected information bit.

V. RESULT

A. Simulation Result

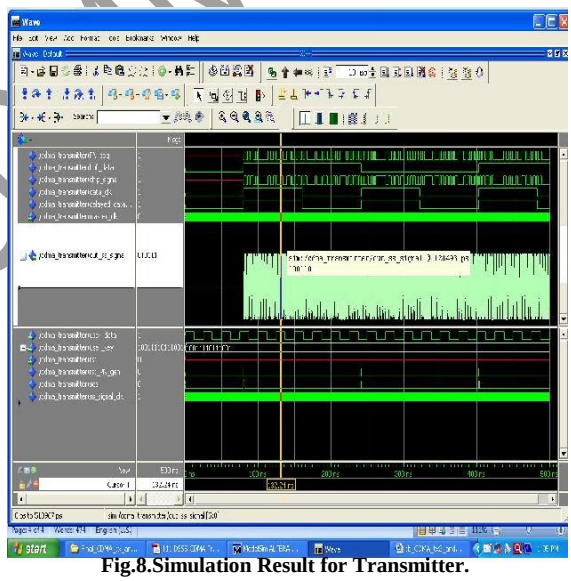

Fig.8.Simulation Result for Transmitter.

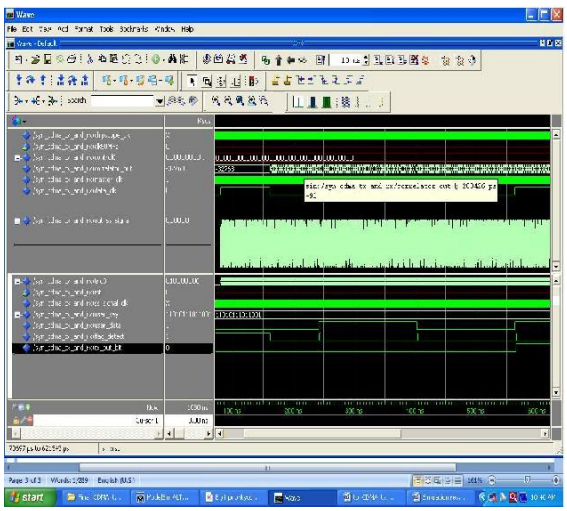

Fig.9. Simulation result for Cdma System.

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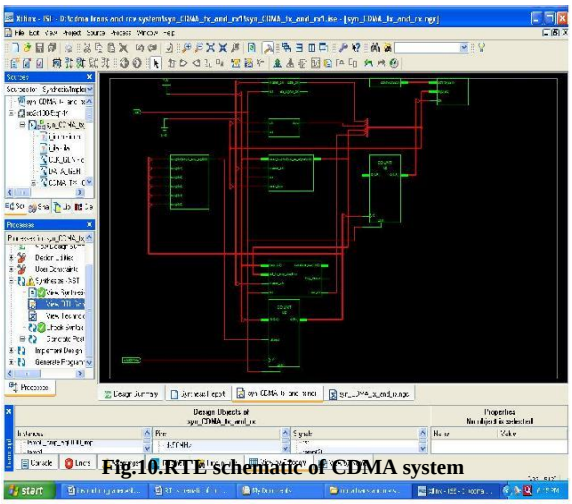

Fig.10.RTE schematic of CDMA system

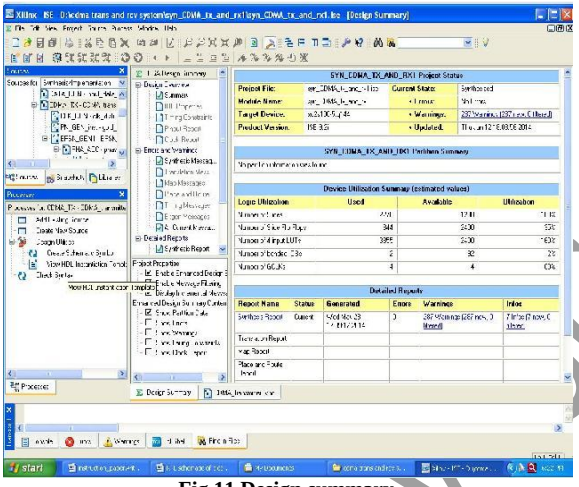

Fig.11.Design summary

In the simulation result we can observe that the received data is same as user data with some amount of delay.

After applying the 14 bit user key 127 bit gold sequence is generated, Synchronization is maintained using buffer logic, start of PN-sequence is indicated by Sos signal, transmitted DS CDMA signal is Out_ss_signal and Flag_detect is raised to 1 whenever a bit is detected.

CONCLUSION

The successful implementation of various modules of DSSS CDMA system is done. It has been observed that the implemented design is fully reconfigurable on any communication links. System developed is implemented with 127 gold code sequence; Implementation with variable length sequence can also be done. The developed DS CDMA system provides efficient area utilization on FPGA. This is obtained by implementing scaling process in receiver section.

FUTURE SCOPE

This project can be further extended to implement multiple transmitters and receiver's system .It can be implemented with different modulation techniques and a comparative analysis can also be made. Various techniques can also be implemented to improve the multipath interference effect. The concept can be extended to design the Global Positioning System which is CDMA system. Frequency hopping spread spectrum technique can also be implemented and compared.

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